TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
(Sample Question)

Exam.	Regular (New Course)		
Level	BE	Full Marks	60
Programme	BEI/BCT	Pass Marks	24
Year / Part	I / II	Time	3 hrs.

Subject: - Digital Logics (EX 152)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1 Convert the followings as indicated: [3×1]
   a. (1101.1011)2 = (?)10
   b. (101101)2 = (?) Grey
   c. (B12.CD7) 16 = (?)8

2 Define an BCD code. Use 1's complement method to perform the following addition (-37 +15)10 in the 16-bit signed number representation. [1+3]

3 Prove the following: [2x2]
   a. $YZ + X(Y \oplus Z) = XZ + Y(X+Z)$
   b. $AB+ BC + \overline{A}\, C = AB + \overline{A}\, C$

4 Simplify the function using K-map $F = \Sigma m (0,1,3,4,7, 8,10,11,12)$ and $d = \Sigma m (2,5, 6,9,15)$. Also realize the simplified circuit using NOR gates only. [4+2]

5 Implement $Y (A, B, C) = \sum m (0, 1, 3, 6, 7)$ using only a single 4:1 DEMUX. Design a circuit which can realize both the full-adder and the full-subtractor in a single circuit. Hints: use mode switch (M). [3+7]

6 Design a 2-bit synchronous Gray code up/down counter using JK flip-flops [7]

7 Explain the operation of 4-bit serial-in parallel-out (SIPO) shift register with necessary circuit and timing diagram for 1101 input data. [3+3]

8 Draw the schematic diagram of three input TTL NAND gate and list the major parameters of CMOS logic family. [4+2]

9 Design a sequential machine that consists of one input, X and one output, Y. The machine gives output high (1), when it detects the sequence 1011 from its input data stream X. [10]

10 Explain the operation of multiplexing display techniques with the help of necessary diagrams and waveforms. [4]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2081 Ashwin

Exam.	**Regular (New Course-2080 Batch)**		
Level	BE	**Full Marks**	60
Programme	BEI, BCT	**Pass Marks**	24
Year / Part	I / II	**Time**	3 hrs.

Subject: - Digital Logic (*EX 152*)

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- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Mention merits and demerits of digital signal over analog signal. [2]
2. Perform the following as indicated: [2×1.5]
   a) (6E.2C)16 = (?)8
   b) (10110110)Gray = (?)2
3. Design the simplest logic circuit for 'f' segment for the BCD-to-seven segment display decoder. [4]
4. Implement Y (A, B, C) = $\sum_m$ (0, 2, 3, 5, 7) using only a single 4:1 MUX. Design a circuit which can realize both the half-adder and the half-subtractor in a single circuit. [3+7]
5. Design a mod-6 synchronous down counter using JK flip-flops. [7]
6. Explain the operation of 4-bit serial-in parallel-out (SIPO) shift register with necessary circuit and timing diagram for input data of1011. [3+3]
7. Describe briefly the operation of 3 bit up/down asynchronous counter having negative edge triggering clock system with neat circuit diagram and timing diagram. [4+3]
8. Design a sequential machine that consists of one input, X and one output, Z. The machine is required to give output high (Y=1), whenever it detects the serial sequence of 101 from its input data stream X. Implement only SR flip-flops for the designed circuit realization. [10]
9. Draw the circuit diagram of two-input TTL NOR gate and explain its logic operation briefly and list the characteristics of CMOS logic family. [5+2]
10. With the help of functional diagram explain the operation of frequency measurement. [4]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2082 Baishakh

Exam.	Back (New Course)		
Level	BE	Full Marks	60
Programme	BCT, BEI	Pass Marks	24
Year / Part	I / II	Time	3 hrs.

Subject: - Digital Logic (*EX 152*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Define an ASCII code. Use 2's complement method to perform the following addition $(-28 + 12)_{10}$ in 8-bit signed number representation. [1+3]
2. Prove the following: [2×2]
   a) $AB + \bar{A}C + BC = AB + \bar{A}C$
   b) $AB + C(A \oplus B) = BC + A(B+C)$
3. What is a decoder? Design an octal priority encoder with neat circuit diagram. [2+6]
4. Realize the following Boolean function using a single 3×8 decoder. Also simplify the logic function implementing K-map method. [3+3]
   $X(A,B,C,D) = \sum_m (0,2,3,7,8,10,11,14,15)$
5. Design a synchronous 2-bit up/down counter using T flip-flops. [7]
6. Explain the operation of 4-bit parallel-in serial-out (PISO) shift register with necessary circuit and timing diagram for 1101 input data. [3+2]
7. Sketch the circuit diagram of mod-12 asynchronous counter having positive-edge triggering clock system implementing JK flip-flops with neat timing diagram. [3+3]
8. Design a sequential machine that consists of one input, X and one output, Z. The machine is required to give output high (Y=1), whenever it detects the serial sequence of 010 from its input data stream X. Implement only D flip-flops for the designed circuit realization. [10]
9. Draw the circuit diagram of two-input CMOS NAND gate and explain its logic operation briefly and list the characteristics of TTL logic family. [4+2]
10. With the help of functional diagram explain the operation of time measuring circuit. [4]

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